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1 Session 45: design/technology interaction: Process variation aware OPC with variational lithography modeling
Peng Yu, Sean X. Shi, David Z. Pan
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(910.89 KB) Additional Information: full citation, abstract, references, index terms

Optical proximity correction (OPC) is one of the most widely used resolution enhancement techniques (RET) in nanometer designs to improve subwavelength printability. Conventional model-based OPC assumes nominal process parameters without considering process variations, due to prohibitive runtimes of lithography simulations across process windows. This is the first paper to propose a true process-variation aware OPC (PV-OPC) framework. It is enabled by the variational lithography modeling and gui ...

Keywords: OPC, lithography modeling, process variation

2 Level set and PDE methods for computer graphics
David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**
Publisher: ACM Press
Full text available: pdf(17.07 MB) Additional Information: full citation, abstract, citings

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

3 Session 45: design/technology interaction: Standard cell characterization considering lithography induced variations
Ke Cao, Sorin Dobre, Jiang Hu
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(642.00 KB) Additional Information: full citation, abstract, references, index terms

As VLSI technology scales toward $65nm$ and beyond, both timing and power performance of integrated circuits are increasingly affected by process variations. In practice, people often treat systematic components of the variations, which are generally traceable according to process models, in the same way as random variations in process corner based methodologies. Consequently, the process corner models are unnecessarily pessimistic. In this paper, we propose a new cell characterization methodolo ...

Keywords: CAD, OPC, RET, design flow, process CD, standard cell

4 A New Methodology for Interconnect Parasitics Extraction Considering Photo-Lithography Effects

Ying Zhou, Zhuo Li, Yuxin Tian, Weiping Shi, Frank Liu

January 2007 **Proceedings of the 2007 conference on Asia South Pacific design automation ASP-DAC '07**

Publisher: IEEE Computer Society

Full text available: pdf(1.15 MB) Additional Information: full citation, abstract

Even with the wide adaptation of resolution enhancement techniques in sub-wavelength lithography, the geometry of the fabricated interconnect is still quite different from the drawn one. Existing Layout Parasitic Extraction (LPE) tools assume perfect geometry, thus introducing significant error in the extracted parasitic models, which in turn cases significant error in timing verification and signal integrity analysis. Our simulation shows that the RC parasitics extracted from perfect GDS-II geo ...

5 Session 7: Lithography and Routing: What's Next? (invited): Research directions for coevolution of rules and routers

Andrew B. Kahng

April 2003 **Proceedings of the 2003 international symposium on Physical design ISPD '03**

Publisher: ACM Press

Full text available: pdf(82.48 KB) Additional Information: full citation, abstract, references, citings, index terms

Design rules in advanced IC manufacturing processes are increasingly problematic for modern router architectures and algorithms. This paper first reviews types and causes of "difficult" design rules, as well as implications for current routing approaches. Next, some basic router components are assessed with respect to future viability. Last, the paper discusses prospects for future "coevolution" of design rules and detailed routing methods.

6 Design methods for manufacturability enhancements: RADAR: RET-aware detailed routing using fast lithography simulations

Joydeep Mitra, Peng Yu, David Z. Pan

June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**

Publisher: ACM

Full text available: pdf(420.43 KB) Additional Information: full citation, abstract, references, cited by, index terms

This paper attempts to reconcile the growing interdependency between nanometer lithography and physical design. We first introduce the concept of lithography hotspots and the edge placement error (EPE) map to measure the overall printability and manufacturing effort. We then adapt fast lithography simulation models to generate EPE map. Guided by EPE map, we develop effective RET-aware detailed routing (RADAR) techniques that can handle full-chip capacity to enhance the overall printability while ...

Keywords: DFM, OPC, RET, detailed routing, lithography

7 A pattern matching algorithm for verification and analysis of very large IC layouts

Mariusz Niewczas, Wojciech Maly, Andrzej Strojwas

April 1998 **Proceedings of the 1998 international symposium on Physical design ISPD '98**

Publisher: ACM Press

Full text available: pdf(922.02 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose a simple, isometry invariant pattern matching algorithm for an effective data reduction useful in layout-related data processing of very complex IC designs. The repeatable geometrical features and attributes are stored in a pattern database. Original pattern instance, or its geometrical attributes, may be quickly regenerated based both on the information stored within the pattern and position of the pattern instance. We also show preliminary results of analysis of the state-of-th ...

8 Data collections and MM: 3D MURALE: a multimedia system for archaeology

John Cosmas, Take Itegaki, Damian Green, Edward Grabczewski, Fred Weimer, Luc Van Gool, Alexy Zalesny, Desi Vanrintel, Franz Leberl, Markus Grabner, Konrad Schindler, Konrad Karner, Michael Gervautz, Stefan Hynst, Marc Waelkens, Marc Pollefeys, Roland DeGeest, Robert Sablatnig, Martin Kampel

November 2001 **Proceedings of the 2001 conference on Virtual reality, archeology, and cultural heritage VAST '01**

Publisher: ACM Press

Full text available: pdf(159.52 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the 3D Measurement and Virtual Reconstruction of Ancient Lost Worlds of Europe system (3D MURALE). It consists of a set of tools for recording, reconstructing, encoding, visualising and database searching/querying that operate on buildings, building parts, statues, statue parts, pottery, stratigraphy, terrain geometry and texture and material texture. The tools are loosely linked together by a common database on which they all have the facility to store and access data. The ...

9 Congestion estimation: Tutorial on congestion prediction

Taraneh Taghavi, Foad Dabiri, Ani Nahapetian, Majid Sarrafzadeh

March 2007 **Proceedings of the 2007 international workshop on System level interconnect prediction SLIP '07**

Publisher: ACM Press

Full text available: pdf(404.16 KB) Additional Information: full citation, abstract, references, index terms

With the increasing sophistication of circuits and specifically in the presence of IP blocks, new estimation methods are needed in the design flow of large-scale circuits. Up to now, a number of post-placement congestion estimation techniques in the presence of IP blocks have been presented. In this paper we present a unified approach for predicting wirelength, congestion and delay parameters early in the design flow. We also propose a methodology to integrate these prediction methods into th ...

Keywords: algorithm, congestion, delay, prediction, wirelength

10 Session 59: panel: DFM: where's the proof of value?

Shishpal Rawat, R. Camposano, A. Kahng, J. Sawicki, M. Gianfagna, N. Zafar, A. Sharan

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(664.70 KB) Additional Information: full citation, abstract, index terms

How can design teams employ new tools and develop response methodologies yet still stay within design budgets? How much effort does it require to be an early adopter and what kind of measurable results compensate for this effort? Panelists discuss how their design-for-manufacture (DFM) tools fit into a fixed design methodology, budget and timeline, and give examples of expected ROI (monetary, quality, reduced time-to-market, and comprehensive yield).The aim of this panel is to provide a serious ...

Keywords: DFM, OPC, RET, ROI, design for manufacture, design for yield, yield optimization

11 Layout design methodolgies for sub-wavelength manufacturing

Michael L. Rieger, Jeffrey P. Mayhew, Sridhar Panchapakesan
June 2001 **Proceedings of the 38th conference on Design automation DAC '01**
Publisher: ACM Press

Full text available: pdf(705.30 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we describe new types of layout design constraints needed to effectively leverage advanced optical wafter lithography techniques. Most of these constraints are dictated by the physics of advanced lithography processes, while other constraints are imposed by new photomask techniques. Among the methods discussed are 1) phase shift mask (PSM) lithography in which phase information is placed to the photomask in combination with conventional clear and dar information; 2) optical p ...

Keywords: OPC, PSM, lithography, optical proximity correction, phase shift mask

12 Process aware physical design: Modeling litho-constrained design layout

Min-Chun Tsai, Daniel Zhang, Zongwu Tang
June 2007 **Proceedings of the 44th annual conference on Design automation DAC '07**
Publisher: ACM Press
Full text available: pdf(207.89 KB) Additional Information: full citation, abstract, references, index terms

This paper derived a method of modeling litho-constrained layout in design stage. The model applies directly on design layout and does not require mask-synthesis steps. Results show we can capture design-relevant litho "hot-spots" within a matter of an hour on a large full-chip data. This method proves that the hot-spot information is embedded in original design layout and can be extracted with strong signal. This method enables a designer to correct real hot-spots before tape-out. It provide ...

Keywords: DFM, OPC, design rules, lithography, modeling, yield

13 Impact of process variations on power: Accurate and efficient gate-level parametric yield estimation considering correlated variations in leakage power and performance

Ashish Srivastava, Saumil Shah, Kanak Agarwal, Dennis Sylvester, David Blaauw, Stephen Director
June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**
Publisher: ACM

Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, references, cited by, index terms

Increasing levels of process variation in current technologies have a major impact on power and performance, and result in parametric yield loss. In this work we develop an efficient gate-level approach to accurately estimate the parametric yield defined by leakage power and delay constraints, by finding the joint probability distribution function

(jpdf) for delay and leakage power. We consider inter-die variations as well as intra-die variations with correlated and random components. The correl ...

Keywords: correlation, leakage, variability, yield

14 Design for manufacturing: Toward a methodology for manufacturability-driven design rule exploration

L. Capodieci, P. Gupta, A. B. Kahng, D. Sylvester, J. Yang

June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**

Publisher: ACM Press

Full text available: pdf(483.26 KB) Additional Information: full citation, abstract, references, citings, index terms

Resolution enhancement techniques (RET) such as optical proximity correction (OPC) and phase-shift mask (PSM) technology are deployed in modern processes to increase the fidelity of printed features, especially critical dimensions (CD) in polysilicon. Even given these exotic technologies, there has been momentum towards less exibility in layout, in order to ensure printability. However, there has not been a systematic study of the performance and manufacturability impact of such a move towards r ...

Keywords: OPC, RET, VLSI manufacturability, lithography, process variation, yield

15 Efficient thee-dimensional extraction based on static and full-wave layered Green's functions

Jinsong Zhao, Wayne W. M. Dai, Sharad Kapur, David E. Long

May 1998 **Proceedings of the 35th annual conference on Design automation DAC '98**

Publisher: ACM Press

Full text available: pdf(306.90 KB) Additional Information: full citation, abstract, references, citings, index terms

In tegral equation approaches based on layered media Green's functions are often used to extract models of integrated circuit structures. The primary advan tage of these approaches over equiv alen t-sourcebased schemes is the dramatic reduction in problem size. When combined with an SVD-accelerated sc heme for the solution of the associated dense linear system, this leads to a substantial speedup. In this paper we deriv e and solve for these multila yered 3D Green's functions usi ...

Keywords: emulation, functional simulation, reconstruction, visibility

16 Statistical Clock Skew Analysis Considering Intra-Die Process Variations

Aseem Agarwal, David Blaauw, Vladimir Zolotov

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design ICCAD '03**

Publisher: IEEE Computer Society

Full text available: pdf(247.70 KB) Additional Information: full citation, abstract, citings, index terms

With shrinking cycle times, clock skew has become an increasinglydifficult and important problem for high performance designs.Traditionally, clock skew has been analyzed using case-files whichcannot model intra-die process variations and hence result in a veryoptimistic skew analysis. In this paper, we present a statistical skewanalysis method to model intra-die process variations. We firstpresent a formal model of the statistical clock skew problem and thenpropose an algorithm which is based on ...

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Advanced topics in physical design: Lens aberration aware timing-driven placement
Andrew B. Kahng, Chul-Hong Park, Puneet Sharma, Qinke Wang
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(220.55 KB) Additional Information: full citation, abstract, references

Process variations due to lens aberrations are to a large extent systematic, and can be modeled for purposes of analyses and optimizations in the design phase. Traditionally, variations induced by lens aberrations have been considered random due to their small extent. However, as process margins reduce, and as improvements in reticle enhancement techniques control variations due to other sources with increased efficacy, lens aberration-induced variations gain importance. For example, our experim ...

18 Session 5: practical applications of DFM: An up-stream design auto-fix flow for manufacturability enhancement
Jie Yang, Ethan Cohen, Cyrus Tabery, Norma Rodriguez, Mark Craig
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(741.41 KB) Additional Information: full citation, abstract, references, index terms

Although many physical limitations have been reached in modern micro-lithography, printed critical dimensions continue to shrink according to the International Technology Roadmap for Semiconductors (ITRS) [1]. To meet the demands imposed by this guideline, the traditional separation between design and manufacturing communities is being bridged. Many EDA tools package manufacturing data for delivery into established simulation engines for design *verification*. However, none of them provide ...

Keywords: DFM, OPC, design flow, layout

19 Information technologies for the 1990s: an organizational impact perspective
Detmar W. Straub, James C. Wetherbe
November 1989 **Communications of the ACM**, Volume 32 Issue 11
Publisher: ACM Press
Full text available: pdf(1.57 MB) Additional Information: full citation, abstract, references, citings, index terms, review

When a thing is new, people say: "It is not true." Later, when its truth becomes obvious, they say: "It is not important." Finally, when its importance cannot be denied, they say: "Anyway, it is not new." Adapted from William James

20 Power considerations at the physical level: Detailed placement for leakage reduction using systematic through-pitch variation
Andrew B. Kahng, Swamy Muddu, Puneet Sharma
August 2007 **Proceedings of the 2007 international symposium on Low power electronics and design ISLPED '07**
Publisher: ACM Press
Full text available: pdf(301.70 KB) Additional Information: full citation, abstract, references, index terms

We present a novel detailed placement technique that accounts for systematic through-pitch variations to reduce leakage. Leakage depends nearly exponentially on linewidth (gate length), and even small variations in linewidth introduce large variability in leakage. A substantial fraction of linewidth variation is systematic with respect to the device layout context. Detailed placement changes context of the devices that are near the cell boundaries and can be used to reduce leakage. Our approa ...

Keywords: aCLV, detailed placement, leakage, lithography, through-pitch

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